Electronic Version
Stylesheet Version v1.1.1

[NONVOLATILE MEMORY STRUCTURE]

Abstract

The invention is directed to a layout of nonvolatile memory device. The memory cell has a gate electrode, a first doped electrode, and a second doped electrode. The first doped electrode is coupled to the bit line. The gate electrode is coupled to one separated word line. A shared coupled capacitor structure is coupled between all of memory cells of the adjacent bit lines from the second doped electrode. The capacitor structure has at least two floating-gate MOS capacitors. Each floating-gate MOS capacitor has a floating-gate transistor having a floating gate, a first S/D region and a second S/D region; and a MOS capacitor coupled to the floating gate. The first S/D region is coupled to the second doped electrode of the corresponding one of the transistor memory cells, and the second S/D region is shared with an adjacent one of the floating-gate transistor.